Viso

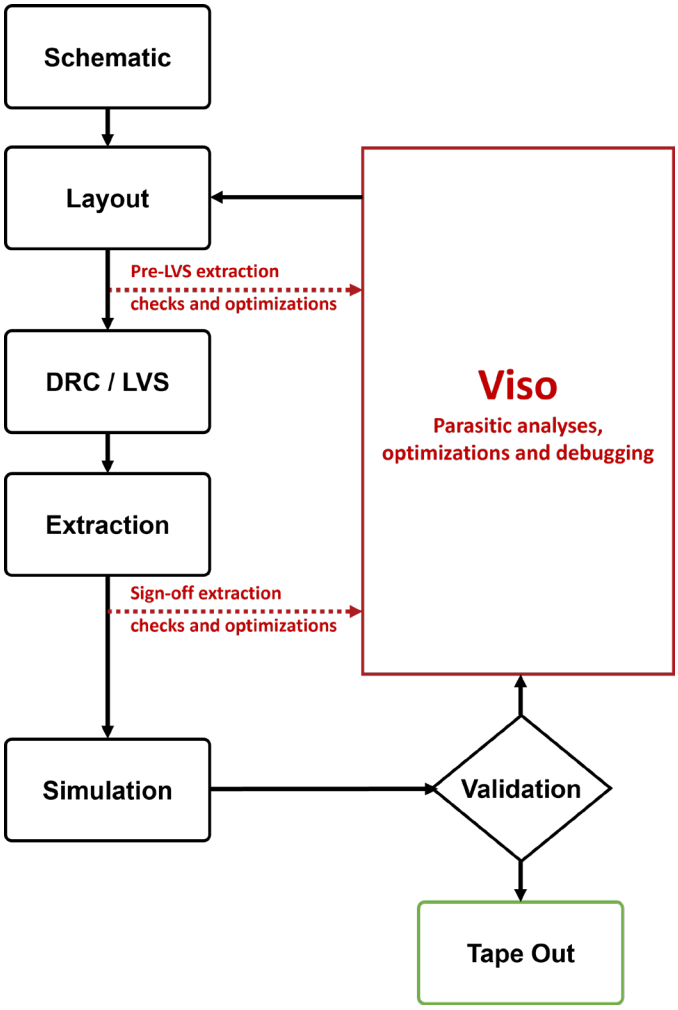
Parasitic Analysis, Exploration, and Debug

SILVACO

Overview

As process geometries grow smaller the number of parasitic elements grow at an exponential rate. The need to manage huge numbers of intricate parasitic elements is propelling the evolution of new design approaches, with the layout now taking on the role of the modern schematic. Meeting this demand involves the development of advanced tools designed to significantly minimize simulation time, foster a comprehensive understanding of parasitic effects, and proactively handle parasitic issues at the earliest stages of the design process.

Viso was developed specifically for this purpose. It facilitates a rapid and comprehensive understanding of parasitic effects that can impact the performance goals of your design. Through robust analyses, Viso addresses various issues such as crosstalk effects, signal weaknesses, unbalanced net symmetries, delays degradation, IR drop problems, and more. Serving as a parasitic-centric analysis and exploration solution, Viso is well-suited to meet the evolving needs of both current and future design requirements.

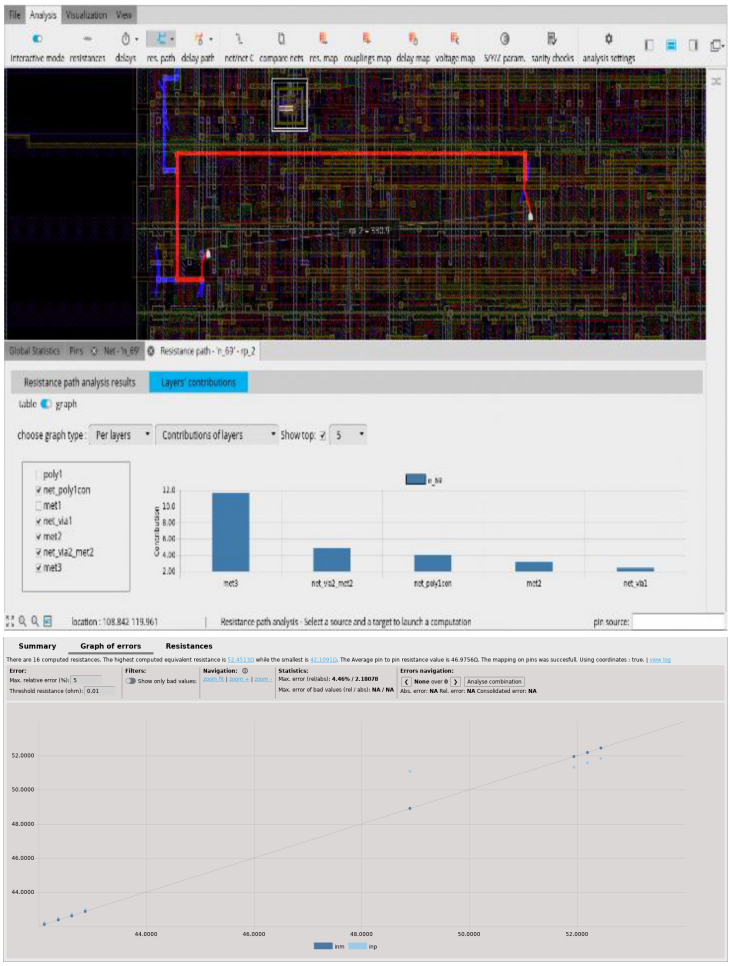


Highlights

- Multiple analyses available
  - Equivalent pin-to-pin resistance per net or across devices (path-tracing)
  - RC delays
  - Crosstalk exploration
  - Access resistance map
  - Voltage map
  - Complex impedance computations
- Highlight of the main contributors responsible for the measured metrics directly on the layout
- Net comparisons with support for differential or parallel signaling
- “What-if” exploratory functionality
- Multifinger pins merging with tunable initial conditions
- Superimposition of GDSII or OpenAccess data over parasitics
- Interactions with Cadence Virtuoso®
- Numerous sanity checks (shortcuts detection, disconnected instances, and more)
- Interactive point and click computations of equivalent resistances and RC delays
- High capacity 2D and 3D rendering capabilities
- Huge capacity, handling over 100 GB netlists and very large power nets

Benefits

- Enables users to spotlight the design of critical and specific nets. With Viso, designers have a fast and easy way to detect potential layout issues early in design, explain where the problems are, and evaluate various solutions.
- Helps to evaluate design performance without running lengthy simulations. Viso calculation runtimes are very fast and can be run on the largest of designs; even designs that were previously considered impossible to simulate.
- Including an extensive set of features, Viso offers many different approaches to assess the quality of a design. Within a few seconds, Viso's sanity check analyses can prevent wasting hours waiting for doomed simulations.
- Allows designers to quickly analyze and optimize very large power networks, either for debug or exploration. Designers can visualize resistance, delay maps and voltage drops without running long and expensive power simulations.
- Intuitive and easy to use with only a parasitic netlist as the required input. Viso can be run either in GUI or command line.



Inputs

- DSPF, SPEF, and SPICE parasitic netlists
- CalibreView parasitic netlists
- OA extracted views

Outputs

- ASCII CSV / TSV results
- Proprietary database for results exploration in the GUI

Platform Support

- Red Hat Enterprise Linux 7.9, 8.X: x86_64
- SLES12 SP5: x86_64

Flows

- GUI
- Command Line Interface

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