Low Power Memory Compiler
1-Port Register File
GF 22nm FDX®

SILVACO

Overview

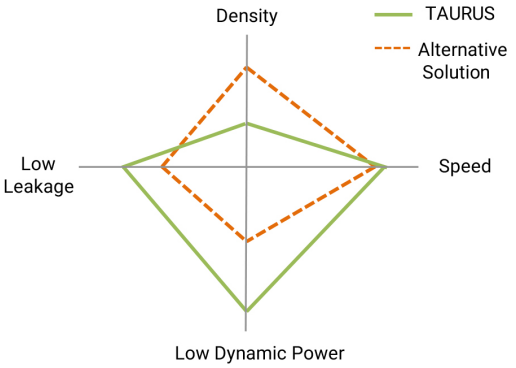
Specifically designed for ultra-low power applications, this memory leverages body biasing to dramatically reduce power consumption.

Highlights

- **Optimized power supply solution**
  - o Active usage of body bias to achieve optimal power and performance
  - o Single rail operation
  - o Operating temperature: -40°C to 125°C
  - o Ultra-wide operating voltage range:
  - ➔[0.5 V +/-10% to 0.8 V +/-10%]
- **FD-SOI optimized**
  - o Tunable performance: power/speed optimization through adaptive or pre-set body biasing
  - o Leakage dramatically lowered due to insulator layer
  - o Lower variability across die due to lower doping effort
- **Optimized architecture**
  - o Custom bitcell enables a wide voltage range
  - o Tunable wakeup time for optimized power/time tradeoff
  - o Multiple modes available for maximum power savings
- **Flexible integration**
  - o Fully functional without Body Biasing
  - o Compatible with any Body Biasing generator
- **Other Features**
  - o Embedded Retention and shut-down switches (optional)
  - o Variable Write Mask

Applications

TAURUS Advantage

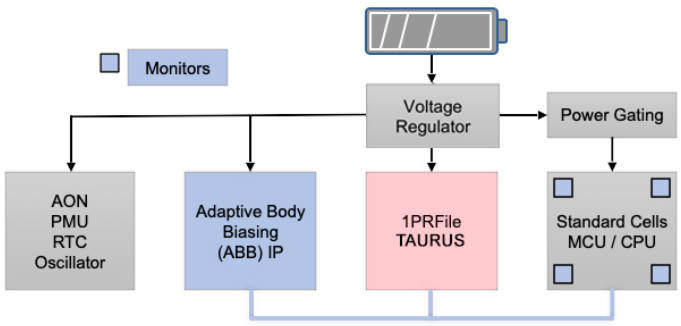


Compiler Specifications

Memory Capacity Range: 128-bits to 40k-bits						
Mux Size	Segments		Address Range	Address Increment Step	Word Width	Word Width Incr. Step
	Num.	Incr. Step				
8	1	-	32-1k	32	4-40	1

Energy Efficient Offering at GF 22nm FDX

- Compatible with industry Adaptive Body Biasing IP for PVT and aging compensation
- Body Biasing functionality (up to +1.3V / -1.5V) to reduce leakage or increase speed at the same power
- Part of the Silvaco GF 22nm FDX IP portfolio



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