Standard Cell Library
Low Voltage Operation
TSMC N3P

SILVACO

Low Voltage SoC Design Challenges

Low Voltage System-on-Chip (SoC) design holds paramount significance in the realm of electronics and semiconductor engineering. The importance of low voltage design lies in its ability to enhance energy efficiency, reduce power consumption, and extend the battery life of electronic devices. As technology advances, the demand for smaller, more portable devices with longer battery life has become increasingly critical. Low voltage SoC design addresses this need by optimizing the power supply voltage to the lowest feasible level without compromising the performance of the integrated circuits. This not only benefits the environment by reducing energy consumption but also caters to the growing market for energy-efficient and sustainable electronic products.

Overview

Silvaco's low voltage Standard Cell Library for the TSMC N3P process represents a breakthrough in power efficiency for high performance SoC designs. A nominal operating voltage of 0.75 V coupled with a low voltage operation of 0.45 V, Silvaco's N3P Standard Cell Libraries enable designers the greatest flexibility in managing the power efficiency for any design.

Highlights

- Nominal voltage of 0.75 V +/-10 %
- Low voltage of 0.45 V +/-10 %
- Track height: 7.5T
- Operating temperature: -40°C to 125°C
- Extensive cell set with fine grained drive strengths
- Optimized for performance and yield with Silvaco tools
- Library augmented with over 150 cells optimized for performance at 0.45 V

Silvaco Standard Cell Libraries for Low Voltage Operation

The challenges of designing a robust Standard Cell Library that can operate at a low voltage is extremely challenging. Ensuring stable and reliable operation, high yields, and robust operating temperature are all essential elements to ensuring your design success. Relying on more than 30 years of low-voltage expertise, Silvaco continues to push the boundaries previously thought unachievable.

Deliverables

Views

- Verilog gate-level
- Liberty Files (timing and power)
- GDSII
- LVS Netlist
- Datasheet

Deliverables

Nominal Voltage

- ffgnp_0p825v_125c_cbest_CCbest_T
- ffgnp_0p825v_m40c_cbest_CCbest_T
- ssgnp_0p675v_125c_cworst_CCworst_T
- ssgnp_0p675v_m40c_cworst_CCworst_T
- tt_0p75v_85c_typical
- tt_0p75v_25c_typical

Low Voltage

- ffgnp_0p44v_125c_cbest_CCbest_T
- ffgnp_0p44v_m40c_cbest_CCbest_T
- ssgnp_0p36v_125c_cworst_CCworst_T
- ssgnp_0p36v_m40c_cworst_CCworst_T
- tt_0p40v_85c_typical
- tt_0p40v_25c_typical

Performance, area, and power specifications are available upon request.

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